INVITATION FOR QUOTATION

No.RIT/TEQIP/FF/Qtn/030/2022

Office of the Principal

Rajiv Gandhi Institute of Technology, Kottayam

Date : 13/06/2022

Sub: RIT-Kottayam –TEQIP – Purchase of FPGA Development Kits under replacement scheme - Quotation- Invited- Reg .

Sealed quotations are invited for the supply of FPGA Development Kits under replacement scheme (a per list attached) in the Electronics and Communication Engineering department specified in the schedu attached below/overleaf. The rates quoted should be for delivery of the item at the place mentioned belo the schedule. The necessary superscription, due date for the receipt of quotations, the date up to which th rates will have to remain firm for acceptance and the name and address of officer to whom the quotation to be sent are noted below. Any quotation received after the time fixed on the due date is liable to b rejected. The maximum period required for delivery of the articles should also be mentioned. Quotation not stipulating period of firmness and with rate variation clause and/or 'subject to prior sale' condition a liable to be rejected.

The rate quoted should be inclusive of all taxes, duties, cesses, etc. which are or may become payable by the contractor under existing or future law or rules of the country of origin/supply or delivery during the course of execution of the contract.

Special conditions, if any, printed on the quotation sheets of the tenders or attached with the tender will not be applicable to the contract unless they are expressly accepted in writing by the purchaser.

Superscription	: Purchase of FPGA Development Kits under replacement scheme
Quotation No.	: No.RIT/TEQIP/FF/Qtn/030/2022
Due date and time for receipt of quotations	: 04/07/2022 11.30 am
Date and Time for opening Quotation	: 04/07/2022 1.30 pm
Date up to which the rates are to remain firm for acceptance	: 31/12/2022
Designation and address of Officer whom the quotation is to be addressed.	: The Principal ,Rajiv Gandhi Institute of Technology, Kottayam

(Authorized Signatory)

PRINCIPAL
RAJIVGANDHI INSTITUTE OF TECHNOLOGY
KOTTAYAM

List of item with specifications

Sl.No.	Item with specifications	Qty
1.	**FPGA Development Kits**:15850 logic slices, each with four 6-input LUTs and 8 flip flops, 4860 kbits of fast block RAM, Six clock management tiles each with PLL ,240 DSP slices, internal clock speeds exceeding 450MHz, On-chip ADC (XADC), Ports and peripherals like 16 user switches USB-UART Bridge , 12-bit VGA output, 3-axi9s accelerometer. 128MiB DDR2, Pmod for XADC signals, 16 user LEDs, Two tri-color LEDs, PWM audio output, Temperature sensor, Serial Flash , Digilent USB-JTAG prt for FPGA programming and communication , Two 4-digit 7 segment displays , Micro SD card connector, PDM microphone ,10/100 Ethernet PHY , Four Pmod ports , USB HID Host for mice, keyboards and memory disks	5 Nos.

Terms & Conditions

1.Rate should be quoted in all items

2.Payment will be made after the satisfactory completion of the supply and verification by the department

(Authorized Signatory)

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